Brijesh Kumar

CONTACT INFORMATION

Department of Electronics and Communication Engg.,
IIT Roorkee, Uttarakhand - 247667 INDIA

Office: +91 1332-284791
e-mail: brijesh@iitr.ac.in

EDUCATION

University of Minnesota, Twin Cities MN, USA
Department of Electrical and Computer Engineering
Doctor of Philosophy January 2010 – July 2013

- Dissertation: Charge Transport in Quantum Dot – Light Emitting Devices
- Advisor: Prof. Stephen A. Campbell (scampbell@umn.edu)
- Co-Advisor: Prof. P. Paul Ruden (ruden@umn.edu)

Master of Science in Electrical Engg. August 2007 – December 2009

- Minor in Nanoparticle Science and Engg.

Indian Institute of Technology (IIT) Delhi, India
Department of Electrical Engineering
Bachelor of Technology July 2003 – July 2007

TECHNICAL SKILLS

Semiconductor Processing: Sputtering, Evaporation, Photolithography, Oxidation, Etch, LPCVD, PECVD.

Characterization: HP Semiconductor Wafer level E-tester, AFM, Surface Profilometer, Ellipsometer, SEM, XPS, AES, XRD, HP parameter analyzer, Optical power meter, Photospectrometer.

Programming: Perl, Fortran, C++, Java, Basic

Software:JMP, SAS, MATLAB, Mathematica, HSPICE, Cadence Virtuoso, LaTeX

WORK EXPERIENCE

Indian Institute of Technology, Roorkee, India

Assistant Professor Apr 2014 – present

Cypress Semiconductor Corporation, Bloomington, MN, USA

Process Development Engineer Sr. Jan 2013 – Jan 2014

- **HP E-tester New Product Support**: Responsible for creating new programs for HP wafer level e-tester.
- **Defect Test-Chip**: Defect test-chip is used to study the defects at individual metal, polysilicon and via layers. It is extremely useful in identifying the root cause of defects and quantifying the improvement with a process change.
- **Wafer warpage reduction**: Due to tensile stress in aluminum, the Si wafers become warped, which makes them difficult to handle using robots. To counter this problem, we are developing a new recipe for ILD layers with increased compressive stress which will balance the tensile stress from metal and hence reduce wafer warpage.
- **TiN metal conversion**: Changing the existing metal stack to an industry standard TiN metal stack to improve yield, reliability and quality.
- **DARC development**: Assisted in development of oxynitride based dielectric anti-reflective coating (DARC) to reduce the reflection of light from metal during photolithography.
- **Photoresist residue defect reduction**: During plasma-phase etch, the photoresist reacts with halides in the plasma to create particles of carbon-based halides, which cause defects in the chips. We are developing an O_2 flash at the end of the etch recipe to oxidize the photoresist particles and thus reduces the defects.

Charge Transport in Quantum Dot – Light Emitting Devices (QD-LED)

Doctoral Research August 2007 – July 2013

- **Fabrication**: Fabricated organic-inorganic hybrid QD-LEDs and demonstrated that two kinds of charge transport mechanism, direct-charge injection and Forster energy transfer, play an important role in these devices.
- **Modeling**: A model for all inorganic QD-LED was developed and the important factors controlling the charge transport in these devices were identified using the model.

Nano-Link: Nanotechnology Resources for Educators

Instructor - Atomic Force Microscopy (AFM) Spring 2010

The primary mission of Nano-Link is to provide nanoscience classroom materials for use by high school and college educators as well as industry. Instructors from various midwest community and technical colleges attended a half day course on AFM taught by me. I also provided them with training on how to use AFM and provided them with samples for their students to practice when they returned to their respective colleges.

Basic Microelectronics Laboratory

Teaching Assistant Fall 2010, 12

Taught a laboratory in which students fabricate a polysilicon gate, single-layer metal, NMOS chip, performing 80 percent of processing, including photolithography, diffusion, oxidation, and etching.

Electronics Laboratory

Teaching Assistant Fall 2011 - Spring 2012

Taught electronics laboratory to non-EE majors in the fall and EE majors in the spring.

Preparation and Characterization of Nanoparticles and Nanowires

B. Tech. Senior Design August 2006 – July 2007

Using chemical vapor deposition (CVD), nanoparticles of tin nitride and nanowires of magnesium oxide were prepared and they were characterized using SEM, TEM and XRD.

Preparation and Surface Characterization of MgO Thin Films

Internship, National Physical Lab, Delhi, India May 2006 – July 2006

Using chemical vapor deposition (CVD), thin films of magnesium oxide were prepared and their depth profile was characterized using XPS.

HONORS AND AWARDS

- 3M Graduate Fellowship August 2008 – May 2012
- Graduate School Fellowship, University of Minnesota August 2007 – May 2008
- Summer Undergraduate Research Award, IIT Delhi May 2005 – July 2005

PUBLICATIONS

- B. Kumar, S.A. Campbell, and P.P. Ruden, **Modeling Charge Transport in Quantum Dot Light Emitting Devices with NiO and ZnO transport layers and Si Quantum Dots**, *Journal of Applied Physics*, 114, 044507 (2013). http://dx.doi.org/10.1063/1.4816680
- B. Kumar, R. Hue, W.L. Gladfelter, and S.A. Campbell, **Comparing direct charge injection and Forster energy transfer into quantum dots in hybrid organic/inorganic quantum dot light emitting devices** , *Journal of Applied Physics*, 112, 034501 (2012). http://dx.doi.org/10.1063/1.4740234
- V.N. Singh, A. Khare, B. Kumar, and B.R. Mehta, **Synthesis of single phase cubic tin nitride nanoparticles by atmospheric pressure-halide vapor phase epitaxy**, *Solid State Sciences*, Volume 10, Issue 5, May 2008, Pages 569-572. http://dx.doi.org/10.1016/j.solidstatesciences.2007.10.007
- V.N. Singh, G. Partheepan, B. Kumar, and A. Khare, **Growth of indium nitride nanopetal structures on indium oxide buffer layer**, *Materials Express*, Volume 3, Number 4, Dec. 2013, Pages 360-364. http://dx.doi.org/10.1166/mex.2013.1132
- B. Kumar, V.N. Singh, A. Khare, and B.R. Mehta, **1-D and 2-D nanostructures of MgO**, *International Workshop on Advanced Materials and Technologies for Nano and Oxide Electronics (AMTNOE) 2007*, New Delhi, India.

RELATED COURSES

Fields and Waves	Engg. Electromagnetics	Engg. Mechanics
Materials Technology	Digital Electronics	IC technology
Materials Characterization	X-Ray Crystallography	Semiconductor Properties and Devices I, II
VLSI Design I	Microelectronics Fabrication	Thin Film Technology
Physics of Semiconductors	Nanostructured materials	Transistor Modeling for Circuit Simulation
Solid State Physics	Quantum Heterostructures	Fluid Mechanics
Semicon. Optoelectronics	Quantum Mechanics	Computational Mechanics